

WHAT IS CLAIMED IS:

1. A one-transistor dynamic random access memory (1T DRAM)

2 device, comprising:

3 a body region insulated from a substrate;

4 an insulating layer on a surface of said body region; and

5 a gate structure on said insulating layer and conformally
6 surrounding a portion of said body region, wherein a width of said
7 body region is sufficient to provide a not fully depleted region.

2. The 1T DRAM device as recited in Claim 1, wherein said

2 width of said body region is greater than a length of said gate
3 structure.

3. The 1T DRAM device as recited in Claim 2, wherein said

2 gate structure is a tri-gate and a ratio of said width of said body
3 region to said gate length is at least about 1.5:1.

4. The 1T DRAM device as recited in Claim 2, wherein said

2 gate structure is a fin-fet and a ratio of said width of said body
3 region to said gate length is at least about 1:1.

5. The 1T DRAM device as recited in Claim 1, wherein said

2 body region is insulated from said substrate by an oxide layer.

6. The 1T DRAM device as recited in Claim 1, wherein said
2 body region is insulated from the substrate by a buried layer of a
3 silicon-on-insulator (SOI) substrate.

7. A method of manufacturing a one-transistor dynamic random
2 access memory (1T DRAM) device, comprising:
3 forming a body region insulated from a substrate;
4 depositing an insulating layer on a surface of said body
5 region; and
6 forming a gate structure on said insulating layer and
7 conformally surrounding a portion of said body region, wherein a
8 width of said body region is sufficient to provide a not fully
9 depleted region.

8. The method as recited in Claim 7, wherein said width of
2 said body region is greater than a length of said gate structure.

9. The method as recited in Claim 8, wherein said gate
2 length is less than about 35 nanometers.

10. The method as recited in Claim 7, wherein said body
2 region is formed from a silicon layer of a silicon-on-insulator
3 (SOI) substrate.

11. The method as recited in Claim 10, wherein forming said
2 body region includes forming a mask by depositing and patterning a
3 resist over said silicon layer and performing an anisotropic etch
4 to remove portions of said silicon layer not protected by said

5 mask.

12. The method as recited in Claim 11, wherein said mask is
2 a sidewall structure.

13. The method as recited in Claim 7, wherein said gate
2 structure is a tri-gate.

14. The method as recited in Claim 13, wherein a ratio of
2 said width of said body region to said gate length is at least
3 about 1.5:1.

15. The method as recited in Claim 7, wherein said gate
2 structure is a FIN-FET.

16. The method as recited in Claim 15, a ratio of said width
2 of said body region to said gate length is at least about 1:1.

17. An integrated circuit, comprising:

2 a one-transistor dynamic random access memory (1T DRAM)

3 device, including:

4 a body region insulated from a substrate;

5 an insulating layer on a surface of said body region; and

6 a gate structure on said insulating layer and conformally

7 surrounding portions of said body region wherein a width of said

8 body region is sufficient to provide a not fully depleted region;

9 a logic transistor located on said substrate; and

10 interconnects to interconnect said 1T DRAM and said logic

11 transistor to form an operative integrated circuit.

18. The integrated circuit as recited in Claim 17, wherein

2 said logic transistor is a multigate transistor having a logic body

3 region, a width of said logic body region being less than said body

4 width of said 1T DRAM device.

19. The integrated circuit as recited in Claim 17, wherein

2 said logic transistor further comprises:

3 a logic body region; and

4 an insulating layer on said surface of said logic body region,

5 wherein said gate structure is on said insulating layer and said

6 gate structure conformally surrounds portions of said logic body

7 region and said gate length is substantially equal to a height and
8 to a width of said logic body region.

20. The integrated circuit as recited in Claim 17, wherein a
2 logic body region of said logic transistor is fully depleted.